



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Swee Yew Choe  
Assignee: Sun Microsystems, Inc.  
Title: HALF-RAIL DIFFERENTIAL DRIVER CIRCUIT  
Serial No.: 10/611,443 Filed: June 30, 2003  
Examiner: Unknown Group Art 2836  
Unit:  
Docket No.: P-9197

Monterey, CA  
November 25, 2003

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER §1.97(b)

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant wishes to call the following documents (a copy of each is enclosed) to the attention of the Examiner:

**U.S. PATENT DOCUMENTS:**

	DOCUMENT NUMBER	DATE	NAME
1)	4,247,791	01/27/81	Rovell
2)	5,859,548	01/12/99	Kong
3)	6,028,454	02/22/00	Elmasry et al.
4)	6,211,704 B1	04/03/01	Kong

**OTHER DOCUMENTS:**

1)	Choe et al., "Dynamic Half Rail Differential Logic for Low Power", IEEE 1997, pages 1936 to 1939
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2)	Jung et al., "Modular Charge Recycling Pass Transistor Logic (MCRPL)", Electronics Letters, 2nd March 2000 Vol. 36 No.5, March 2, 2000, Pages 404 to 405
3)	Kong et al., "Charge Recycling Differential Logic for Low-Power Application", ISSC96 secession 18, IEEE 0-780331962/98, 1998, Pages 302 to 448
4)	Choe et al., "Half Rail Differential Logic", ISSCC97/Secession 25/Processors and Logic/Paper SP 25.6 IEEE 0-7803-3721-2/97, 1997, pages 420 to 421, 336 to 337 and 489
5)	Won et al., "Modified Half Rail Differential Logic for Reduced Internal Logic Swing", IEEE 0-7803-4455-3/98, 1998, pages II-157 to II-160
6)	Kong et al., "Charge Recycling Differential Logic (CRDL) for Low-Power Application", IEEE Journal of Solid-State Circuits, Vol. 31, No. 9, September 1996, pages 1267 to 1276

A PTO form 1449 listing these documents is enclosed.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

If the USPTO issued a first office action prior to the mailing date of this paper, the Commissioner is hereby authorized to charge any fees required for consideration of this Information Disclosure Statement, and to credit any overpayment of fees to Deposit Account No. 50-0553.

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on November 25, 2003.

Respectfully submitted,



Attorney for Applicant

Philip J. McKay  
Attorney for Applicant  
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November 25, 2003  
Date of Signature

Form PTO-1449

Atty Docket No.

Serial No.

P-9197

10/611,443

Applicant(s)

Swee Yew Choe

Filing Date

June 30, 2003

Group

2836

**INFORMATION DISCLOSURE CITATION  
IN AN APPLICATION**

(Use several sheets if necessary)

**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	4,247,791	01/27/81	Rovell	307	238	
	AB	5,859,548	01/12/99	Kong	326	113	
	AD	6,028,454	02/22/00	Elmasry et al.	326	115	
	AC	6,211,704 B1	04/03/01	Kong	326	121	
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

**FOREIGN PATENT DOCUMENTS**

							Translation	
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	YES	NO
	AL							
	AM							
	AN							
	AO							
	AP							

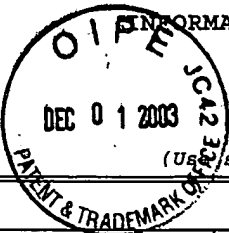
**OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	Choe et al., "Dynamic Half Rail Differential Logic for Low Power", IEEE 1997, pages 1936 to 1939
	AS	Jung et al., "Modular Charge Recycling Pass Transistor Logic (MCRPL)", Electronics Letters, 2nd March 2000 Vol. 36 No.5, March 2, 2000, Pages 404 to 405
	AT	Kong et al., "Charge Recycling Differential Logic for Low-Power Application", ISSC96 secession 18, IEEE 0-780331962/98, 1998, Pages 302 to 448

Examiner

Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

Form PTO-1449				Atty Docket No. P-9197		Serial No. 10/611,443		
<div style="text-align: center;">  <p>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</p> <p>(Use several sheets if necessary)</p> </div>				Applicant(s) Swee Yew Choe				
				Filing Date June 30, 2003		Group 2836		
<b>U.S. PATENT DOCUMENTS</b>								
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
	AA							
	AB							
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<b>FOREIGN PATENT DOCUMENTS</b>								
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	AS	Won et al., "Modified Half Rail Differential Logic for Reduced Internal Logic Swing", IEEE 0-7803-4455-3/98, 1998, pages II-157 to II-160						
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